USER MANUAL

Accessory 8D Option 7

Resolver To Digital Converter Board

307-0ACC85-xUxx

September 1, 2004

DELTA TAU
Data Systems, Inc.
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INTRODUCTION

PMAC's ACC-8D Option 7 (P/N 307-0ACC8D-OPT) is a printed circuit board for resolver-to-digital conversion. This board provides up to four channels of resolver inputs to the PMAC controller. The inputs may be used as feedback or master reference signals for the PMAC servo loops. The basic configuration of the board contains two 12-bit fixed resolution tracking resolver-to-digital (R-to-D) converters. Option A adds another two converters and Option B provides a rail mount stand. The tracking converters used in this accessory are the AD2S90 monolithic converters manufactured by Analog Devices that have the specifications outlined below.

AD2S90 Specification

Parameters	Min	Typical	Max	Units
Converter Dynamics				
Bandwidth	700	840	1000	Hz
Maximum Tracking Rate	375			rps
Settling Time				
1^{o} Step		5		ms
179^{o} Step		20		ms
Accuracy				
Angular Accuracy			+/- 9	LSB*
Repeatability **			1	LSB
* 1 LSB = 5.3 arc minute. ** Specified at constant temperature.				

For more information on the converter's specifications, refer to the AD2S90 Data Sheet available from Analog Devices at:

Analog Devices
One Technology Way
P.O. Box 9106,
Norwood, MA 02062-9106
Tel: (617) 329-4700

ACC-8D Option 7 can interface to most industry standard resolvers. Typical resolvers requiring 5 to 10 kHz excitation frequencies with voltages ranging from 5 to 10V peak-to-peak are compatible with this PMAC accessory. Provisions are made for three on-board generated excitation signals (2.44, 4.88 and 9.76 kHz). In addition, the user may choose to bring into the board an external excitation input. Adjustment pots are provided so that, depending on a particular resolver's rotor to stator winding ratio, the sine and the cosine signals' magnitude are optimized for R-to-D conversion (5V peak-to-peak).

Note:

3-phase synchros are not compatible with this accessory.

For the standard single stage resolvers, up to four R-to-D converters (one ACC-8D Option 7 with Option A) may be interfaced to the basic 4-axis PMAC controller. All versions of PMAC with Option 1 can handle eight R-to-D converters (two ACC-8D Option 7 with Option A). For PMAC-VME and PMAC-PC, using the Axis Expansion accessory (ACC-24), eight additional channels (16 in total) of R-to-D converters may be interfaced to a single PMAC (up to four ACC-8D Option 7s with Option A).

For geared resolvers, up to three R-to-D converters may be used for each feedback channel of PMAC. This means that up to 48 R-to-D converters (3*16) can be connected to a single 8-axis PMAC supported by an eight-channel Axis Expansion board (ACC-24 with Option 1).

CONNECTORS

Refer to the layout diagram of the ACC-8D Option 7 for the location of the connectors on the board. A pin definition listing for each connector is outlined in this manual.

J1A (JTHW)

This is a 26-pin header that provides the link between PMAC's JTHW (J3) and the R-to-D board through the supplied flat cable. Through this connector, PMAC captures the absolute resolver position.

J1B (JTHW)

This is a 26-pin header that brings out the JTHW signals for the next accessory board on the JTHW multiplex memory map. This connector is pin-to-pin compatible with J1A.

JENC1

This is a 10-pin header that provides a convenient means to feedback the emulated A QUAD B and C encoder signals generated by the first R-to-D converter. One of the supplied 10-pin flat cables may be used to connect this header with ACC-8D's J1A, J2A, J3A, or J4A headers.

Note:

For single stage resolvers, the choice of which JxA header to use would depend on the user's selection of routing for the emulated A QUAD B encoder signals to a particular PMAC encoder channel. For geared resolvers, the finest resolution encoder should be connected to J1A via JENC1.

JENC2 to JENC4

These are 10-pin headers that duplicate the function of JENC1 for the second to the fourth R-to-D converters respectively.

TB1

This is a 26-pin terminal block (13-pin on a two-channel board) which is used for the connection of the actual resolvers to this board. Three separate twisted pair shielded cables should be used for each resolver: one for the rotor and two for the stators connections (see the recommended wiring schematic).

TB2

This is a 26-pin terminal block (13-pin when ordered without Option A) which brings out the emulated A QUAD B and C encoder signals from the R-to-D converter board (this connector may be used as an alternative to the JENC connectors). These signals must be routed to the appropriate PMAC encoder channels on the JMACH connectors. This may be conveniently done via the terminal block accessory (ACC-8D). Also, if none of the JENC connectors are used, a 5 volt power supply for the digital logic circuits associated with the on board opto-isolation circuitry should be brought in through this connector.

TB3

This is a 6-pin terminal block through which the analog power supplies for the R-to-D converters are brought in. In addition, an optional external excitation signal for the resolvers may be brought in through this connector.

Note:

For external excitation, pins 1 and 2 of E1 should be jumpered.

MULTIPLEX ADDRESS MAP

ACC-8D Option 7 generates both absolute and incremental position data from resolvers. Normally, the absolute position is read (by PMAC) only upon the power up sequence. The incremental (emulated A QUAD B) data is counted continuously. In order to read the absolute position, the Thumbwheel Port (JTHW) of PMAC is used. Up to two ACC-8D Option 7 boards may be read by PMAC at the same address on the JTHW multiplex memory space. The most significant seven bits of the 8-bit DIP switch, SW1, determine the address of one (or two) particular boards. Although this memory space is 8-bits wide, each ACC-8D Option 7 requires only one nibble (4 bits) of data for the absolute position reading. The least significant bit of SW1 (switch 1) determines whether the low or the high nibble is used. As a consequence, two ACC-8D Option 7 boards may occupy the same two bytes of the address space provided that the SW1 switch 1 is set differently on each board.

When geared resolvers are used on a motor, all of the resolvers for that motor must be connected to R/D converters at the same multiplex address.

SW1 Dip Switch Setting For Board Address *

Multiplex Address	Least significant 16-bits of Ix10 & Ix81	SW1 Dip Switch Setting						
		8	**7**	**6**	**5**	**4**	**3**	**2**
0-1	($0100)***	ON**	ON**	ON**	ON**	ON**	ON**	ON**
2-3	($0002)	ON	ON	ON	ON	ON	ON	OFF
4-5	($0004)	ON	ON	ON	ON	ON	OFF	ON
6-7	($0006)	ON	ON	ON	ON	ON	OFF	OFF
8-9	($0008)	ON	ON	ON	ON	OFF	ON	ON
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
246-247	($00F6)	OFF	OFF	OFF	OFF	ON	OFF	OFF
248-249	($00F8)	OFF	OFF	OFF	OFF	OFF	ON	ON
250-251	($00FA)	OFF	OFF	OFF	OFF	OFF	ON	OFF
252-253	($00FC)	OFF	OFF	OFF	OFF	OFF	OFF	ON
254-255	($00FE)	OFF	OFF	OFF	OFF	OFF	OFF	OFF

This table shows the DIP switch setting for various base addresses of the board:

* SW1 switch 1 allows the addressing of two R-to-D converter boards at the same multiplex address (the same DIP switch setting for SW1 bits 2 to 8). Setting SW1 switch 1 ON directs the absolute position data to the low nibble of the Thumbwheel port (locations 0 to 3). Setting SW1 switch 1 OFF directs the absolute position data to the high nibble of the Thumbwheel port (locations 4 to 7). If SW1 Switches 2 to 8 are the same on two separate R-to-D boards, then SW1 switch 1 should be set differently on each board.

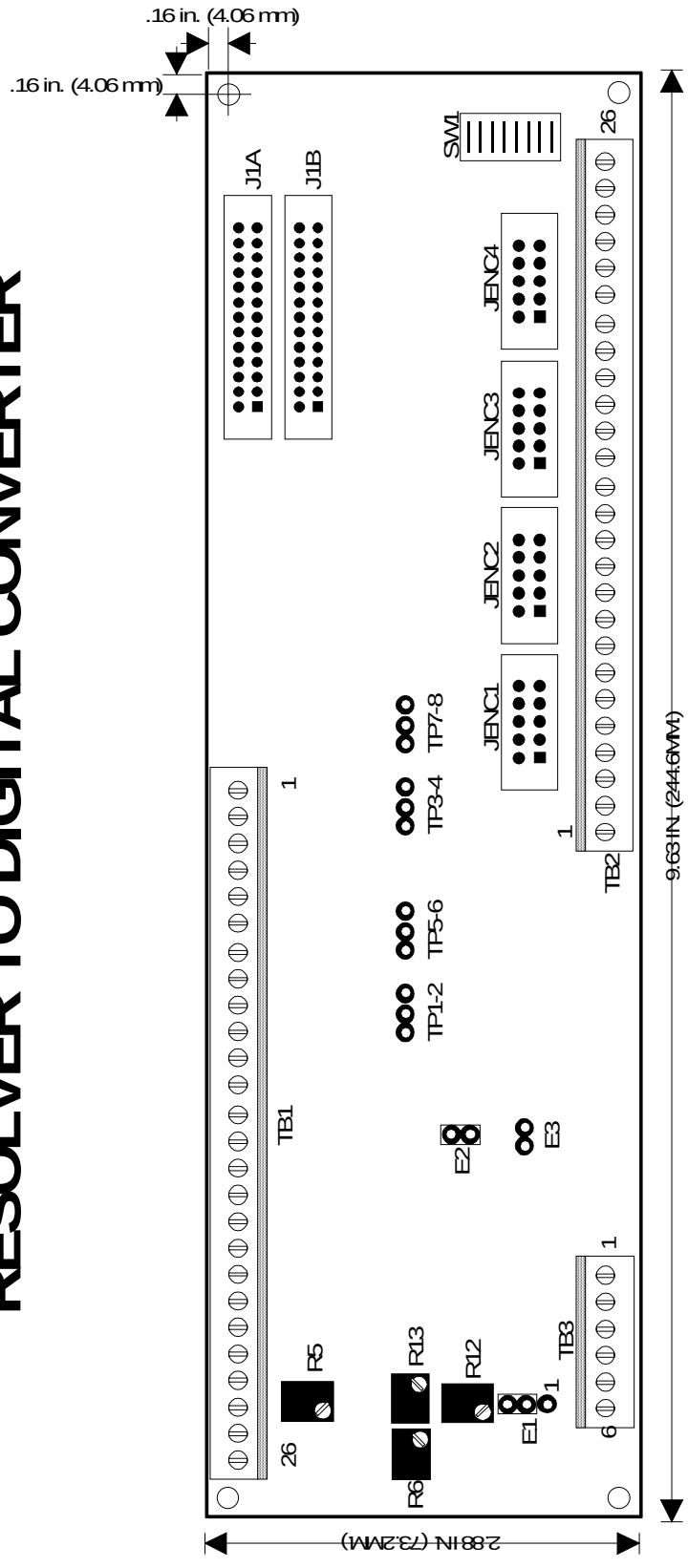
** Default factory setup has SW1 switches 2 to 8 all ON. SW1 switch 1 is also ON. This means that, by default, the board is address decoded for bytes 0 &1 on the multiplex address map. Also the two (four with Option A) R-to D converters occupy locations 0 and 1 (0 to 3 with Option A).

*** Because the use of an address value of $0000 in parameters of Ix10 and Ix81 disables the power on read function, an address value of $0100 (256) should be used to represent multiplex addresses 0 & 1.

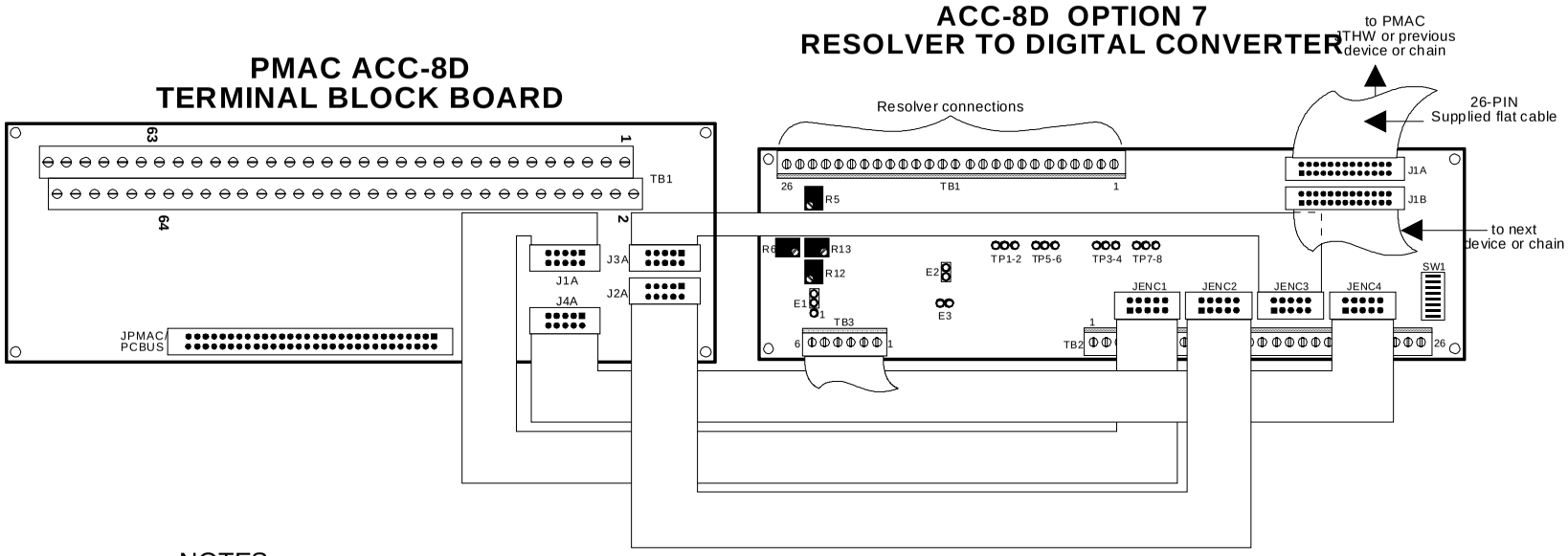
The next table shows the role of DIP switch SW1 for selecting the low and the high nibbles in a particular multiplex address.

The R-to-D Converter Locations for the Absolute Position Read in Relation to the Incremental Position Read

Location	DIP Switch SW1 Switch 1 Setting	Absolute Resolver Position Read From	Incremental Resolver Position Read Through
0 (On first board at a given multiplex address)	ON	Resolver connected to TB1 pins 1 to 6	JENC1 or TB2 pins 1 to 6
1 (On first board at a given multiplex address)	ON	Resolver connected to TB1 pins 7 to 12	JENC1 or TB2 pins 7 to 12
2 (On first board at a given multiplex address)	ON	Resolver connected to TB1 pins 13 to 18	JENC1 or TB2 pins 13 to 18
3 (On first board at a given multiplex address)	ON	Resolver connected to TB1 pins 19 to 24	JENC1 or TB2 pins 19 to 24
4 (On Second board at a given multiplex address)	OFF	Resolver connected to TB1 pins 1 to 6	JENC1 or TB2 pins 1 to 6
5 (On Second board at a given multiplex address)	OFF	Resolver connected to TB1 pins 7 to 12	JENC1 or TB2 pins 7 to 12
6 (On Second board at a given multiplex address)	OFF	Resolver connected to TB1 pins 13 to 18	JENC1 or TB2 pins 13 to 18
7 (On Second board at a given multiplex address)	OFF	Resolver connected to TB1 pins 19 to 24	JENC1 or TB2 pins 19 to 24


ACC-8D OPTION 7
RESOLVER TO DIGITAL CONVERTER
.16 in. (4.06 mm)
.16 in. (4.06 mm)
J1A
J1B
SW1
JENC1
JENC2
JENC3
JENC4
TP1-2
TP3-4
TP5-6
TP7-8
TB1
TB2
TB3
E1
E2
E3
R5
R6
R12
R13
2.88 IN (73.2MM)
9.63 IN (244.6MM)

Connecting ACC-8D Option 7 To PMAC via the Terminal Block



NOTES:

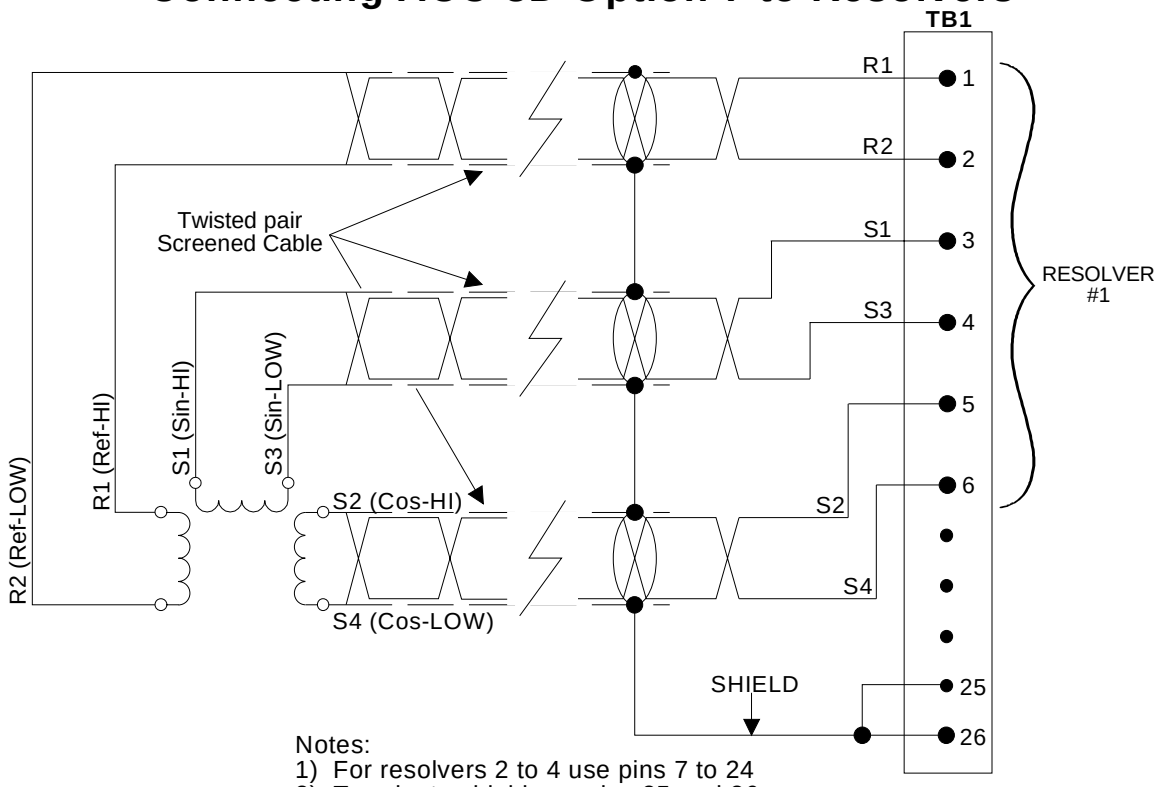
1) TB2 may be used instead of JENCX headers when discrete wires are being used.

2) For non-geared resolvers, any JENCX (X=1 to 4) may be connected to any JXA (X=1 to 4)

3) For two geared resolvers use JENC1 and JENC2 pair or JENC3 and JENC4 pair. (see manual for instructions)

4) For three geared resolvers use JENC1, JENC2 and JENC3. (see manual for instructions)

Connecting ACC-8D Option 7 to Resolvers



Notes:
1) For resolvers 2 to 4 use pins 7 to 24
2) Terminate shields on pins 25 and 26

PMAC I-VARIABLE SETUP

If no power-on absolute position information is desired from any of the resolvers, then the ACC-8D Option 7 simply acts as a resolver-to-quadrature converter. If this is the case, then PMAC I-variable setup is exactly the same as for incremental encoders and this section can be ignored.

The following I-Variables are specifically implemented in PMAC firmware version 1.14 and above for the operation of ACC-8D Option 7 (refer to the PMAC User Manual for a detailed description of their functions):

I8x	Motor x Third-Resolver Gear Ratio
I9x	Motor x Second-Resolver Gear Ratio
Ix10	Motor x Power-On Servo Position Address
Ix75	Motor x Power-On Phase Position Offset
Ix81	Motor x Power-On Phase Position Address

In addition, the TWR form of M-variables (available in firmware versions 1.14 and above) has been specifically implemented for ACC-8D Option 7.

SETUP FOR SINGLE-STAGE RESOLVERS

It is assumed that the necessary physical connections between the resolver and ACC-8D Option 7 are properly implemented. Moreover, the ACC-8D Option 7 and the PMAC board must be connected via JTHW. Finally, ACC-8D Option 7's emulated A QUAD B signals must be brought into one of PMAC's JMACH encoder inputs (usually through ACC-8D). Refer to the connection diagram enclosed with this manual.

Example: To connect a single-stage resolver, which is hard-wired into ACC-8D Option 7 channel 1 (TB 1 pins 1 to 6), into PMAC's feedback channel one, connections should be as follows:

1. Connect the supplied 26-pin flat cable between ACC-8D Option 7's J1 to PMAC's JTHW connector.
2. Connect one of the supplied 10-pin flat cables between ACC-8D Option 7's JENC1 header and ACC-8D's J1A. You may follow the same procedure for the single-stage resolvers two to four (i.e. connect JENC2 ... JENC4 to J2A ... J4A respectively).

Note:

For single-stage resolvers, any of the four resolver channel on the Option 7 board may be connected to any encoder input channel on the ACC-8D board (i.e. the order is not critical).

3. Inspect and (if necessary) modify the SW1 DIP switches such that the multiplex address of the board does not conflict with other accessory boards using the JTHW port.

If PMAC is not using the resolver for commutation purposes, then all you need to set is Ix10 for Motor x Power-On Servo Position Address. This I-variable's numerical value consists of two parts. The low 16 bits contain the address of the register containing the power-on position data, either a PMAC memory I/O address, or an address on the multiplexer (Thumbwheel) port. The high eight bits specify how to read the information at this address. For resolvers interfaced to PMAC via ACC-8D Option 7, the most significant bit (bit 23) of Ix10 determines the interpretation of the numerical value of the absolute position. If Ix10 bit 23 is 0, the value read from the absolute sensor is treated as an unsigned quantity. If the most significant bit is 1, which adds $80 to the high eight bits of Ix10, the value read from the sensor is treated as a signed two's complement quantity. Bits 16 to 21 must contain a value from 0 to 7. The address specified in the low 16 bits is a multiplexer port address with a valid range of $0002 to $0100 (2 to 256 decimal), evenly divisible by 2. (See the R-to-D Converter Locations table, and note that the actual multiplexer port address ranges from 0 to 254, but in Ix10, a value of 256 must be used to represent address 0). The value in the high eight bits specifies the location of the resolver at a particular multiplex address. With SW1 switch 1 in the ON position, the locations are 0 to 3. With SW1 switch 1 in the OFF position, the locations are 4 to 7. For the above example, if the SW1 switches are set at the factory default (see the R-to-D Converter Locations table), then the resolver would be addressed at location 0 of the R-to-D converter board at multiplex address zero and I110=$000100 for unsigned binary interpretation and I110=$800100 for two's complement interpretation ($100=256 decimal, representing multiplex address zero). Refer to the PMAC User's Manual for more examples and a more detailed description of Ix10.

Note:

The encoder decode I-variables I900, I905, .., I975 must be set to 7 for x4 quadrature decode, CCW (e.g. I900=7 for encoder 1). This setting enables the direction of incremental encoder count up/down to agree with the direction of the absolute position read from the R-to-D converter. To have the CW rotation count up (or down), swap the Sine output of the resolver with the Cosine output at TB1. Furthermore, if the polarity of the DAC output does not match the polarity of the resolver for negative feedback (i.e. a positive Open loop command such as `O10`, generates a negative velocity), then one must physically change the polarity of the DAC signal to the amplifier.

If PMAC is (additionally) using the resolver for commutation of a brushless dc motor, it is possible to set up the PMAC such that the need for the standard phase finding procedure is eliminated. This is an attractive feature made possible by the fact that the resolver provides absolute (as opposed to incremental) angular position data. Two I-variables need to be set up properly to perform phasing from a resolver. Ix81 must be set to contain the address and the format of the resolver. If Ix81 is greater than zero, PMAC will read from the specified address in the specified format on power-up/reset to get the absolute position data. Ix75 specifies the difference between the sensor's zero position and the phase cycle's zero position in units of counts*Ix70. After reading the power-up/reset position data from the R-to-D converter board, PMAC adds this value and writes the resulting sum to the phase position register.

ABSOLUTE PHASING FOR COMMUTATION

Note:

The phase finding initialization instruction described below is a setup procedure, which is best, carried out with a motor/resolver combination disconnected from any motor load (inertia or otherwise). Decouple the motor/resolver sub-system from the load prior to the execution of the following procedure.

To set up for absolute phasing, it is necessary to initially carry out a standard phasing search routine using the stepper motor method implemented in a PLC program or with on-line commands from the host computer. All of the instructions for setting up the commutation with an incremental encoder apply here (see PMAC User Manual). Repeat the power-on phasing procedure several times to make certain that the results are consistent (i.e. the motor moves in both direction with small open loop commands) (e.g. `O5`, `O-5`).

To determine the phasing offset required for automatic power-on phasing, it is necessary to define an M-variable to read the resolver absolute position through the Thumbwheel port. This is a TWR form of an M-variable. Example:

```
M171->TWR:0,0           ;Resolver at multiplexer address 0, location 0
```

Next, it is necessary to run the stepper motor phasing search, using on-line commands. This action forces the motor into the zero point of the phasing cycle. At this point, the absolute position should be read using the TWR format M-variable.

Example: Suppose Motor 1 is a brushless DC which is connected to a resolver and is required to be set up for absolute position phasing:

The exact sequence depends on the value of Ix72.

For Ix72 = 64 (4-phase) or 85 (3-phase):

```
#1O0                    ;Open loop command with zero magnitude
I129=-2000 I179=2000    ;For motor to a preliminary position
I129=0                  ;Now force motor to zero-point of phase cycle
```

For Ix72 = 192 (4-phase) or 171(3-phase):

```
#1O0                    ;Open loop command with zero magnitude
I129=2000 I179=-2000    ;For motor to a preliminary position
I129=0                  ;Now force motor to zero-point of phase cycle
```

At this point, the absolute position is read by querying the M-variable value. **Example:**

```
M171        ;ask for the value of M171
475         ;PMAC responds
```

This value should be *negated*, multiplied by Ix70, and then stored in Ix75. **Example:** If I170=1, then the following on-line command must be issued:

```
I175=-475*I170
```

Finally, Ix81, the Motor x Power-On Phase Position Address I-variable must be set to point to the correct R-to-D input. Ix81 should be set to point to the correct address within the multiplexer address space. Similar to Ix10, the least significant 16 bits of Ix81 should contain the Thumbwheel multiplex address of the R-to-D converter and the most significant eight bits must contain the location number within a given address (0 to 7). For the above example:

I181=$000100

To complete the initialization process for power-on phasing via resolvers, the following steps must be taken:

1. Remove phase bias by typing **Ix79=0 & Ix29=0**
2. Disable automatic phasing search by setting **Ix73=0 & Ix74=0**
3. If it is desired that the motor be immediately enabled upon power-up, **Ix80=1**
4. Type the **SAVE** command.

At this stage, one should be able to issue the $ motor-rephase command. If the phasing works well, one should be able to move the motor easily in both directions with small open-loop (e.g. O10) commands. If the motor appears to lock up in one or both directions, Ix81 should be set to zero and the stepper motor method of phasing should be repeated again.

SETUP FOR GEARED RESOLVERS

ACC-8D Option 7 may be used for interfacing with geared resolvers. Through PMAC I-variables (I8x and I9x), provisions are made for the absolute power-on read of up to three geared resolvers. For a detailed description of these I-variables, refer to the PMAC User Manual.

For three stage-geared resolvers, one Option 7 board is required, which must be populated with its Option A (must have at least three R-to-D converters, the fourth converter on the board may be used for a single stage resolver). For two-stage geared resolvers, the basic ACC-8D Option 7 board, which is populated with two R-to-D converters, is adequate.

Note:

For two-stage geared resolvers, the fine resolver must be connected physically to the lower numbered R-to-D converter input (must be TB1 pins 1 to 6 or TB1 pins 13 to 18). The coarse resolver must be connected to the next higher numbered R-to-D converter input on the same board (must be TB1 pins 7 to 12 or TB1 pins 19 to 24).

For three-stage geared resolvers, the fine resolver must be physically connected to the lowest numbered R-to D converter input (must be TB1 pins 1 to 6). The intermediate resolver must be connected to the next higher numbered R-to-D converter input on the same board (must be TB1 pins 7 to 12), and the coarse resolver must be connected to next higher number R-to-D converter on board (must be TB1 pins 13 to 18).

In either case, (two- or three-stage geared resolvers) one only needs to connect the incremental A QUAD B output from the fine resolver converter to the PMAC via JENCx or TB2.

I8x is the gear ratio between the second (medium) and the third (coarse) resolvers for a three-stage geared resolver system. With a numerical range of 0 to 4095, the ratio is the number of turns the second resolver makes in one full revolution of the third resolver. This parameter is used only during PMAC's power-up/reset cycle to establish absolute power-on servo position. This parameter must be saved via the **SAVE** command and the PMAC card reset before it takes effect. If there is no geared third resolver for Motor x, or if absolute power-on position is not desired, I8x should be set to zero. If either Ix10 (for the fine resolver) or I9x (for the intermediate resolver) is set to zero, I8x is not used.

Example: Motor 1 has a three-stage resolver, with each resolver geared down by the ratio of 24:1 from the next finer resolver. The fine resolver is connected to the R-to-D converter at location 4 at the multiplexer address 2 (the first R-to-D converter on the second ACC-8D Option 7 at address 2). The intermediate resolution resolver should be at location 5 and the coarse resolver at location 6. The following I-variable setting should be used:

```
I110=$040002            ;The 0002 in the low 16 bits specifies
                        ;multiplexer address 2
                        ;the 04 in the high 8 bits specifies
                        ;converter location 4
                        ;absolute position treated as an unsigned number.
```

or

```
I110=$840002            ;The 0002 in the low 16 bits specifies
                        ;multiplexer address 2
                        ;the 04 in the high 8 bits specifies
                        ;converter location 4
                        ;absolute position treated as a 2's
                        ;complement number
I91=24                  ;Specifies 24:1 ratio between intermediate
                        ;and fine
I81=24                  ;Specifies 24:1 ratio between coarse and
                        ;intermediate
```

I9x is the gear ratio between the primary (fine) and the secondary resolvers for a two- or a three-stage geared resolver system. With a numerical range of 0 to 4095, it is the number of turns the fine resolver makes in one full revolution of the second resolver. This parameter is used only during PMAC's power-up/reset cycle to establish absolute power-on servo position. This parameter must be saved via the **SAVE** command and the PMAC card reset before it takes effect. If there is no geared second resolver for Motor x, or if absolute power-on position is not desired, I9x should be set to zero. If Ix10 (for the fine resolver) is zero then neither I9x (for the intermediate resolver) or I8x (for coarse resolver) are used.

Example: Motor 1 has a two-stage resolver, with the coarse resolver geared down by the ratio of 16:1 from the fine resolver. The fine resolver is connected to the R-to-D converter at location 0 at the multiplexer address 0 (the first R-to-D converter on the first ACC-8D Option 7 at address 0). The coarse resolver should be at location 1. The following I-variable setting should be used:

```
I110=$000100            ;The 0100 in the low 16 bits specifies
                        ;multiplexer address 0
                        ;the 00 in the high 8 bits specifies
                        ;converter location 0
                        ;absolute position treated as an unsigned number.
```

or

```
I110=$800100            ;The 0100 in the low 16 bits specifies
                        ;multiplexer address 0
                        ;the 00 in the high 8 bits specifies
                        ;converter location 0
                        ;absolute position treated a 2's complement number.
i91=16                  ;Specifies 16:1 ratio between coarse and fine
i81=0                   ;Specifies third geared resolver not installed
```

OPTIONAL EXTERNAL EXCITATION

An excitation signal with a peak-to-peak magnitude not more than 10V may be supplied externally to all the resolvers on the same board via TB3 (note that the sine and the cosine signals should not be more than 5 volts peak-to-peak). Jumper E1 should be set between pins 1 and 2. This signal should be sinusoidal and its frequency may range from 2 kHz to 10 kHz depending on the resolvers needs.

For the internally generated rotor excitation signal, E1 should be jumpered between pins 2 and 3. Jumpers E2 and E3 determine the excitation frequency as follows:

E3	E2	Internal Excitation Frequency (kHz)
OFF	OFF	2.44
OFF	ON	4.88 (default)
ON	ON	9.76

ANALOG TEST POINTS AND POTS

Test points TP7 and TP8 and the pot R5 are associated with the R-to-D converter 1. TP3 and TP4 and the pot R6 are associated with R-to-D converter 2. TP5 and TP6 and the pot R12 are associated with R-to-D converter 3. And TP1 and TP2 and the pot R13 are associated with R-to-D converter 4. For each channel, the test points may be used to monitor the sine and the cosine signals from the resolvers. The peak-to-peak voltage should be approximately 5V. If the peak-to-peak signal magnitude is not approximately 5V, then the corresponding pot may be adjusted accordingly.

POWER SUPPLY AND OPTO-ISOLATION CONSIDERATIONS

The power for the PMAC processor side of the opto-isolation circuitry (+5V supply) is brought in directly from J1 (JTHW). The power for the emulated A QUAD B signal drivers (+5V supply) is either brought in through JENCx connectors or the terminal block TB2. The current requirement is less than 350 mA. For a fully populated board, the power for the analog side of the opto-isolation circuitry, which is brought in through the terminal block TB3, is 300 mA for the +15 V supply, and 250 mA for the -15V supply.

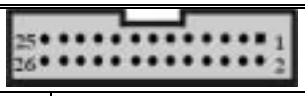
Power Requirements

5V	12V	-12V	Other 24V etc.
350mA	300mA	250mA	N/A

CONNECTOR PINOUTS

Headers and Terminal Blocks

J1A (26-Pin Header)

Top View 

Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Output	Data Bit 0	*
4	SEL0	Input	Address Line 0	**
5	DAT1	Output	Data Bit 1	*
6	SEL 1	Input	Address Line 1	***
7	DAT2	Output	Data Bit 2	*
8	SEL2	Input	Address Line 2	***
9	DAT3	Output	Data Bit 3	*
10	SEL3	Input	Address Line 3	***
11	DAT4	Output	Data Bit 4	*
12	SEL 4	Input	Address Line 4	***
13	DAT5	Output	Data Bit 5	*
14	SEL5	Input	Address Line 5	***
15	DAT6	Output	Data Bit 5	*
16	SEL6	Input	Address Line 6	***
17	DAT7	Output	Data Bit 6	*
18	SEL7	Input	Data Bit 7	***
19	N.C.			Not connected
20	GND	Common	PMAC Common	
21	N.C.			Not connected
22	GND	Common	PMAC Common	
23	N.C.			Not connected
24	GND	Common	PMAC Common	
25	+5V	Input	+5V DC Supply	
26	N.C.			Not connected

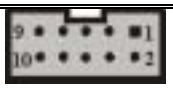
* These outputs are used for the serial transmission of absolute position data from the R-to-D board to PMAC (one line per channel). Depending on the position of SW1 switch 1, each R-to-D board occupies either the DAT0 to DAT3 or DAT4 to DAT7. R-to-D converters 1 to 4 are mapped respectively to DAT0 to DAT 3 (locations 0 to 3) if SW1 switch 1 is ON. R-to-D converter 1 to 4 is mapped respectively to DAT4 to DAT7 (locations 4 to 7) if SW1 switch 1 OFF.

** SEL0 is used to clock out the serial transmission of absolute position from all converters.

*** These input lines are used to address the R-to-D board by PMAC.

J1A is a 26-pin header that provides the link between PMAC's JTHW (J3) and the R-to-D board through the supplied flat cable. Through this connector, PMAC captures the absolute resolver position.

JENC1 (10-Pin Header)

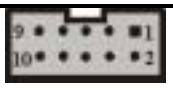
Top View 

Pin #	Symbol	Function	Description	Notes
1	CHA1	Output	A Channel	H.P. Standard
2	+5V	Input	Power Supply	H.P. Standard
3	GND	Common	Digital Ground	H.P. Standard
4	CHA1/	Output	Negative A Channel	Added
5	CHB1/	Output	Negative B Channel	Added
6	GND	Common	Digital Ground	H.P. Standard
7	+5V	Input	Power Supply	H.P. Standard
8	CHB1	Output	B Channel	H.P. Standard
9	+5V	Input	Power Supply	H.P. Standard
10	CHC1	Output	C Channel	H.P. Standard

JENC1 is a 10-pin header that provides a convenient means for the feedback for the emulated A QUAD B and C encoder signals generated by the first R-to-D converter. One of the supplied 10-pin flat cables may be used to connect this header with ACC-8D's J1A, J2A, J3A, or J4A header.

Note: The choice of which JxA header to use would depend on the user's selection of routing for the emulated A QUAD B encoder signals to a particular PMAC encoder channel.

JENC2 (10-Pin Header)

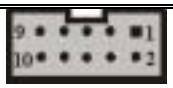
Top View 

Pin #	Symbol	Function	Description	Notes
1	CHA2	Output	A Channel	H.P. Standard
2	+5V	Input	Power Supply	H.P. Standard
3	GND	Common	Digital Ground	H.P. Standard
4	CHA2/	Output	Negative A Channel	Added
5	CHB2/	Output	Negative B Channel	Added
6	GND	Common	Digital Ground	H.P. Standard
7	+5V	Input	Power Supply	H.P. Standard
8	CHB2	Output	B Channel	H.P. Standard
9	+5V	Input	Power Supply	H.P. Standard
10	CHC2	Output	C Channel	H.P. Standard

JENC2 is a 10-pin header that provides a convenient means for the feedback for the emulated A QUAD B and C encoder signals generated by the second R-to-D converter. One of the supplied 10-pin flat cables may be used to connect this header with ACC-8D's J1A, J2A, J3A, or J4A header.

Note: The choice of which JxA header to use would depend on the user's selection of routing for the emulated A QUAD B encoder signals to a particular PMAC encoder channel.

JENC3 (10-Pin Header)

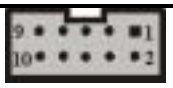
Top View 

Pin #	Symbol	Function	Description	Notes
1	CHA3	Output	A Channel	H.P. Standard
2	+5V	Input	Power Supply	H.P. Standard
3	GND	Common	Digital Ground	H.P. Standard
4	CHA3/	Output	Negative A Channel	Added
5	CHB3/	Output	Negative B Channel	Added
6	GND	Common	Digital Ground	H.P. Standard
7	+5V	Input	Power Supply	H.P. Standard
8	CHB3	Output	B Channel	H.P. Standard
9	+5V	Input	Power Supply	H.P. Standard
10	CHC3	Output	C Channel	H.P. Standard

JENC3 is a 10-pin header that provides a convenient means for the feedback for the emulated A QUAD B and C encoder signals generated by the third R-to-D converter. One of the supplied 10-pin flat cables may be used to connect this header with ACC-8D's J1A, J2A, J3A, or J4A header.

Note: The choice of which JxA header to use would depend on the user's selection of routing for the emulated A QUAD B encoder signals to a particular PMAC encoder channel.

JENC4 (10-Pin Header)

Top View 

Pin #	Symbol	Function	Description	Notes
1	CHA4	Output	A Channel	H.P. Standard
2	+5V	Input	Power Supply	H.P. Standard
3	GND	Common	Digital Ground	H.P. Standard
4	CHA4/	Output	Negative A Channel	Added
5	CHB4/	Output	Negative B Channel	Added
6	GND	Common	Digital Ground	H.P. Standard
7	+5V	Input	Power Supply	H.P. Standard
8	CHB4	Output	B Channel	H.P. Standard
9	+5V	Input	Power Supply	H.P. Standard
10	CHC4	Output	C Channel	H.P. Standard

JENC4 is a 10-pin header that provides a convenient means for the feedback for the emulated A QUAD B and C encoder signals generated by the fourth R-to-D converter. One of the supplied 10-pin flat cables may be used to connect this header with ACC-8D's J1A, J2A, J3A, or J4A header.

Note: The choice of which JxA header to use would depend on the user's selection of routing for the emulated A QUAD B encoder signals to a particular PMAC encoder channel.

TB1 (13 or 26-pin Terminal Block)

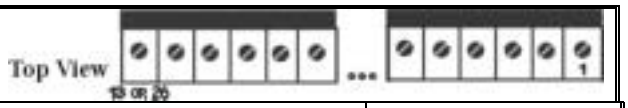
Pin #	Symbol	Function	Description	Notes
1	R1-1	Output	Ref. 1 High	*
2	R2-1	Output	Ref. 1 Low	*
3	S1-1	Input	Sine 1 High	**
4	S3-1	Input	Sine 1 Low	**
5	S2-1	Input	Cosine 1 High	**
6	S4-1	Input	Cosine 1 Low	**
7	R1-2	Output	Ref. 2 High	*
8	R2-2	Output	Ref. 2 Low	*
9	S1-2	Input	Sine 2 High	**
10	S3-2	Input	Sine 2 Low	**
11	S2-2	Input	Cosine 2 High	**
12	S4-2	Input	Cosine 2 Low	**
13	R1-3	Output	Ref. 3 High	*
14	R2-3	Output	Ref. 3 Low	*
15	S1-3	Input	Sine 3 High	**
16	S3-3	Input	Sine 3 Low	**
17	S2-3	Input	Cosine 3 High	**
18	S4-3	Input	Cosine 3 Low	**
19	R1-4	Output	Ref. 4 High	*
20	R2-4	Output	Ref. 4 Low	*
21	S1-4	Input	Sine 4 High	**
22	S3-4	Input	Sine 4 Low	**
23	S2-4	Input	Cosine 4 High	**
24	S4-4	Input	Cosine 4 Low	**
25	AGND	Analog Common	Shield	
26	AGND	Analog Common	Shield	

*Jumpers E1, E2, and E3 determine the source and the frequency of the resolver excitation frequency. This is a differential signal pair. Use a shielded twisted pair cable, connect shield to terminal pin 25 or 26.

**This is a differential signal pair. Use a shielded twisted pair cable, connect shield to terminal pin 25 or 26.

TB1 is a 26-pin terminal block (13-pin on a two channel board) which is used for the connection of the actual resolvers to this board. Use three separate twisted pair shielded cables for each resolver: one for the rotor and two for the stators connections (see the recommended wiring schematic).

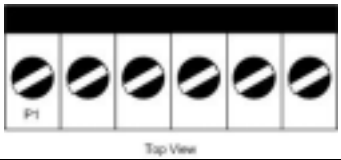
TB2 (13 or 26-pin Terminal Block)



Pin #	Symbol	Function	Description	Notes
1	CHA1	Output	Enc. 1 A Chan.	
2	CHA1/	Output	Enc. 1 Negative A Channel	
3	CHB1	Output	Enc. 1 B Chan.	
4	CHB1/	Output	Enc. 1 Negative B Channel	
5	CHC1	Output	Enc. 1 C Chan.	
6	CHC1/	Output	Enc. 1 Negative C Channel	
7	CHA2	Output	Enc. 2 A Chan.	
8	CHA2/	Output	Enc. 2 Negative A Channel	
9	CHB2	Output	Enc. 2 B Chan.	
10	CHB2/	Output	Enc. 2 Negative B Channel	
11	CHC2	Output	Enc. 2 C Chan.	
12	CHC2/	Output	Enc. 2 Negative C Channel	
13	CHA3	Output	Enc. 3 A Chan.	
14	CHA3/	Output	Enc. 3 Negative A Channel	
15	CHB3	Output	Enc. 3 B Chan.	
16	CHB3/	Output	Enc. 3 Negative B Channel	
17	CHC3	Output	Enc. 3 C Chan.	
18	CHC3/	Output	Enc. 3 Negative C Channel	
19	CHA4	Output	Enc. 4 A Chan.	
20	CHA4/	Output	Enc. 4 Negative A Channel	
21	CHB4	Output	Enc. 4 B Chan.	
22	CHB4/	Output	Enc. 4 Negative B Channel	
23	CHC4	Output	Enc. 4 C Chan.	
24	CHC4/	Output	Enc. 4 Negative C Channel	
25	+5V	Input	Digital Power Supply	
26	GND	Common	Digital Ground	

TB2 is a 13-pin or a 26-pin terminal block (13-pin for two R-to-D converters and 26-pin for four). This terminal block brings out the emulated A QUAD B and C encoder signals from the R-to-D converter board. (This connector may be used as an alternative to the JENC connectors.)
The signals must be routed to the appropriate PMAC encoder channels on the JMACH connectors. This may be done via the Terminal Block accessory (ACC-8D). Also, if none of the JENC connectors are used, a 5V power supply for the digital logic circuits associated with the on-board opto-isolation circuitry should be brought in through this connector.

TB3 (6-Pin Terminal Block)



Pin #	Symbol	Function	Description	Notes
1	AGND	Common	Analog Ground	
2	A+15V	Input	+15V Supply	
3	AGND	Common	Analog Ground	
4	A-15V	Input	-15V Supply	
5	AGND	Common	Analog Ground	
6	EXTREF	Input	External Resolver Excitation Input	Optional; E1-1 should be jumpered to E1-2.

TB3 is a 6-pin terminal block through which the analog power supplies for the R-to-D converters are brought in. In addition, an optional external excitation signal for the resolvers may be brought in through this connector. (For external excitation, jumper pins 1 and 2 of E1.)